30 Gbps, Broadly Tunable, All-Optical, Clock Recovery Circuit

K. Vlachos, G. Theophilopoulos, A. Hatziefremidis, H. Avramopoulos
Department of Electrical and Computer Engineering,
National Technical University of Athens, 15773 Zographou, Athens, Greece
tel: +30-1-772 2076, fax: +30-1-772 2077, email: hav@cc.ece.ntua.gr

Summary

The ability to generate locally, a high quality optical clock signal from a jittered data stream, is necessary for the realization of ultra high capacity WDM/TDM transmission and all-optical processing systems [1,2]. In particular clock recovery, is extremely important for the design and demonstration of relatively high functionality, multi-gate, ultra-high speed, all-optical digital logic circuits, as it may allow the synchronization of the optical signals between remote processing units. Optical clock recovery circuits have been demonstrated using a semiconductor optical amplifier (SOA) in an EDFA ring laser [3], the Kerr effect in optical fiber [4], a self pulsating two section DFB laser diode [5,6] and a figure of eight laser [7,8].

In the present communication we demonstrate a simple, fully pigtailed circuit containing a single SOA as the active device, capable of recovering clock from a data pattern up to 30 Gbps and generating a 2.7 ps clock pulse train with very low modulation pattern. The recovered clock signal has been investigated for pseudo-random data sequences generated from a bit error rate test (BERT) set and periodic data patterns with special attention to very long sequences of consecutive 0's. The circuit used here for clock recovery, is a mode-locked, fiber ring oscillator that uses a single SOA device both as the gain and modulator elements [9]. The optical data stream enters the clock recovery oscillator and modulates the gain of the SOA forcing it to mode-lock. Use of a single SOA device in a fiber oscillator, ensures that the repetition rate at which the circuit may recover clock is adjustable, it is broadly wavelength tunable, nearly polarization insensitive and relatively simple to build.

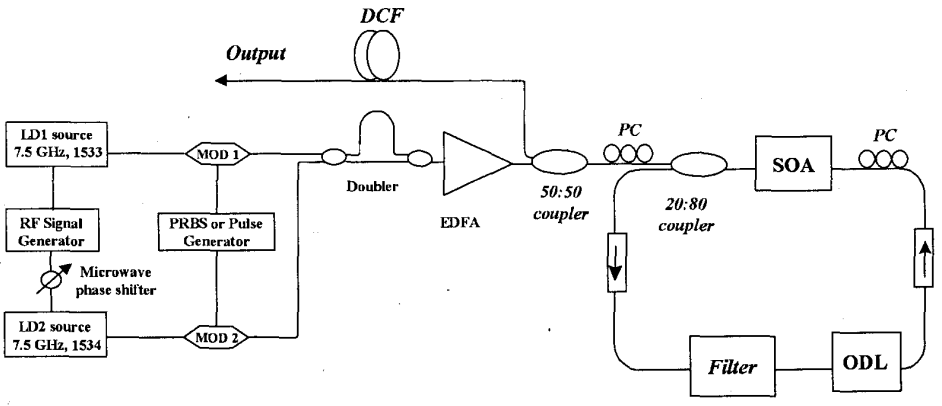

Fig.1 Experimental setup of clock recovery circuit

Fig. 1 shows the experimental layout. The clock recovery circuit was constructed entirely from fiber-pigtailed devices. Gain is provided by a 500 μm, bulk InGaAsP/InP ridge waveguide SOA, which had a

peak gain at 1535-nm and could provide 23 dB small signal gain with 250 mA dc drive current. As the SOA exhibited 2 dB polarization gain dependence, a polarization controller was introduced at its input port. Faraday isolators were used in the oscillator to ensure unidirectional operation and to stop the data pattern from circulating in the ring. A 20% fused optical fiber coupler was used to insert the data stream into the ring cavity and to extract the recovered clock signal. Wavelength selection was achieved with a tunable, 5 nm band pass filter. In order to tune the repetition frequency of the clock recovery circuit to that of the data stream, a variable optical delay line (ODL) was used. The total linear loss of the cavity was 10 dB.

The 30 Gbps test data patterns were generated from two DFB laser diodes each gain switched at 7.5 GHz, operating at 1533 nm and 1534 nm. The pulse trains from the two diodes were next linearly compressed with dispersion compensating fiber (DCF) to yield 7 ps and were each modulated in lithium niobate modulators, driven at 7.5 Gbps from the synchronized channels of a BERT pattern generator or a programmable pulse generator. The patterns from each diode were bit interleaved to 15 Gbps and repetition frequency doubled to 30 Gbps using a split-relatively-delay-and-recombine fiber doubler. Before insertion into the clock recovery circuit, the data pattern was amplified in an EDFA capable of delivering up to 1 mW of average power into the ring and the polarization state of the incoming data pattern was adjusted for best performance. With the ODL adjusted so that the fundamental frequency of the fiber ring is a harmonic of the line frequency of the data pattern, the oscillator generates mode-locked pulse trains with low output modulation. The output pulses were monitored on a second harmonic autocorrelator and found to be 6 ps long and not-transform limited. These pulses were subsequently compressed to 2.5 ps with DCF of –14.25 ps/nm total dispersion. The pulsewidth-bandwidth product of the compressed pulses was 0.34, very close to that of a squared hyperbolic secant profile.

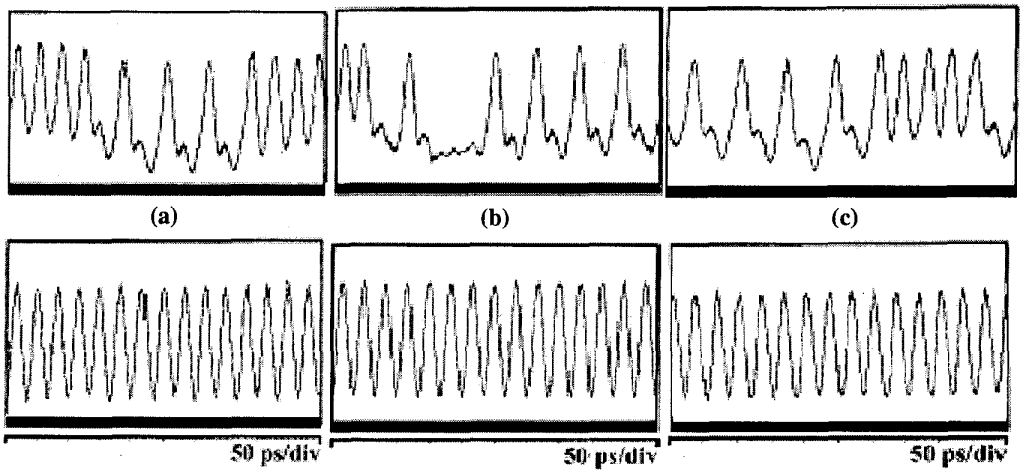

Fig.2 Data pattern (upper row) and recovered clock (lower row) for (a) 2^7-1, (b) 2^{10}-1 and (c) 2^{15}-1, PRBS data sequences.

Figs 2 (a), (b) and (c) show samples of the PRBS data sequences with length 2^7-1, 2^{10}-1 and 2^{15}-1 respectively (upper row) and the recovered clock (lower row), showing negligible output modulation pattern. The recovered clock was also monitored on a 40 GHz microwave spectrum analyzer and revealed suppression of the clock rate subharmonics in excess of 40 dB with respect to the recovered clock signal. Fig 3 (a) shows the variation of the output pulse width and the modulation pattern imposed on the recovered clock signal across its wavelength tuning range for 2^{10}-1 PRBS pattern. The circuit generates nearly transform limited pulses that are within 6% of 2.7 ps and provides approximately constant output

power of 70 μW across its 20 nm tuning range. The output modulation pattern directly from the clock recovery circuit was less than 8%. As the mode-locking process of this clock recovery circuit is based on the fast gain dynamics of the SOA, the main concern on its operation is the possibility of strong modulation pattern on the recovered clock signal when the input data stream contains very long sequences of consecutive 0's.

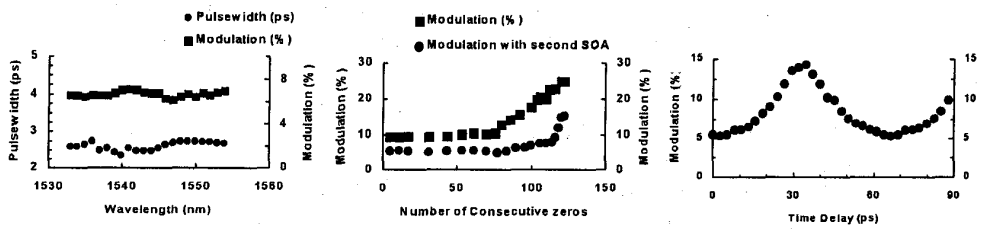

Fig.3 (a) Pulsewidth and output modulation pattern change against wavelength for the 30 GHz recovered clock for 2^{10}-1 input PRBS. (b) Output modulation pattern change of 30 GHz recovered clock against the number of consecutive zeros, directly from circuit and with additional SOA at its output and (c) Modulation pattern variation against relative delay between the two 15 Gbps PRBS sequences

To investigate this the modulators were driven with a two-channel programmable pulse generator. Fig 3 (b) shows as an example, the variation of the output modulation as the number of consecutive 0's increases for a data pattern with 125 MHz repetition period. This figure shows that for 72 consecutive 0's the pattern is less than 10 %. Even though 10% modulation on the recovered clock is acceptable for such long series of consecutive 0's, this can be improved substantially if a second SOA is used at the output of the clock recovery circuit. Fig 3(b) also shows that the addition of the second SOA virtually removes completely any remaining modulation pattern and shows that for 100 consecutive 0's the pattern is 6 %. Finally the effect of mistiming between the two 15 Gbps PRBS data patterns from the two diodes, was investigated. It was found that even if the two patterns are mistimed by one full bit period, the clock recovery circuit still recovers clock at 30 GHz however with an increased modulation pattern. Fig 3 (c) shows the variation of the recovered clock pattern as the relative delay between the two patterns is varied.

In summary we have demonstrated a simple and robust clock recovery circuit. The circuit has been evaluated up to 30 Gbps and has been shown to produce stable, nearly transform limited pulse trains of 2.7 ps duration width, across a 20 nm tuning range. The quality of the recovered clock signal has been exhaustively examined and shows that the circuit produces clock signal with less that 10 % modulation even in the presence of a 36 consecutive 0's. It has also been shown that the addition of a separate SOA at the output of the circuit reduces the modulation pattern to 6% even for 50 consecutive 0's.

References

1. K.L. Hall and K.A. Rauschenbach, Opt. Lett. **23**, 1271 (1998).
2. J.P. Sokoloff, P.R. Pruncal, I. Glesk and M. Kane, IEEE Photon. Technol. Lett. **5**, 787 (1993).
3. D.M. Patrick and R.J. Manning, Electron. Lett. **30**, 151 (1994).
4. A.D. Ellis, K. Smith and D.M. Patrick, Electron. Lett. **29**, 1323 (1993).
5. U. Feiste, D.J. As and A. Ehrhardt, IEEE Photon. Technol. Lett. **6**, 106 (1994).
6. B. Sartorius, C. Bornholdt, O. Brox, H.J. Ehrke, D. Hoffmann, R. Ludwig and M. Mohrle, Electron. Lett. **34**, 1664 (1998).
7. L.E. Adams, E.S. Kintzer and J.G. Fujimoto, Electron. Lett. **31**, 1759 (1995).
8. S. Bigo and E. Desurvire, Electron. Lett. **31**, 1855 (1995).
9. T. Papakyriakopoulos, K. Vlachos, A. Hatziefremidis, H. Avramopoulos, Opt. Lett. **24**, 1209 (1999).